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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,681	09/22/2003	Noriyasu Sakai	14225-022001 / F1030476US	9392

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EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/667,681	SAKAI ET AL.	
	Examiner	Art Unit	
	Scott Geyer	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7,8 and 11-13* is/are rejected.

7)☒ Claim(s) *3,5,6,9,10 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The amended drawings received on July 11th, 2005 are acceptable.

Specification

The amendments to the specification received on July 11th, 2005 are acceptable.

Claim Objections

The amendments to claims 7 and 9 received on July 11th, 2005 are acceptable.

Claim Rejections - 35 USC § 112

The amendment to claim 2 received on July 11th, 2005 is acceptable - - accordingly, the rejection of claim 2 under 35 USC 112 (second paragraph) is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 7, 8 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashida et al. (6,767,767 B2) in view of Lee et al. (5,924,190).

As to **claim 1**, Hayashida et al. teach a method of forming an encapsulated semiconductor chip according to first and third embodiments, which are described by figures 1-19 and 21 (see also column 6, line 25 et seq.). Circuit elements (i.e. chips) 10 are attached to a planar body (i.e. substrate) 20. The substrate has conductive patterns as shown by the more detailed figure 6B (which is the encapsulated chip after the molding step). Multiple chips are attached to a substrate and encapsulated as evidenced by figure 1. Also, the chips are disposed on the conductive mounting portions as seen in figure 21 (i.e. flip-chip mounting instead of wire bonding. Wire bonding is shown in the first embodiment as shown in figure 6B; flip-chip bonding is shown in the third embodiment as shown in figure 21). A lower mold 30B and upper mold 30A are brought together around the chips-on-substrate structure as shown in figure 1, and the upper mold has an air vent 37. An insulating resin (i.e. encapsulating resin) 8 flows into the mold to encapsulate the chips. The chips are then separated to form the product as shown by figure 6A-6B (see also figures 7-19, especially figures 18-19). Hayashida et al. do not teach the lower mold having an air vent. However, Lee et al. teach a similar chip molding method wherein both the upper mold and the lower mold halves have air vents (see figures 1, 3, 6,11 or 14). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Hayashida et al. with a mold having air vents in the upper and lower mold portions, as taught by Lee et al. so as to allow for total air escape from both the top and bottom surfaces of the article being molded, which would also reduce or eliminate unwanted air pockets (see also Lee et al., col. 1, lines 65-67, continued to col. 2, lines 1-4).

As to **claim 2**, Hayashida et al. teach blocks formed by a plurality of mounting portions arranged in a matrix form, and resin sealing is performed to cover all this chips that are arranged in matrix form on the blocks (see figures 1, 2 and 21).

As to **claim 4**, Hayashida et al. teach a planar body (i.e. a chip substrate) that has multi-layered conductive patterns laminated with an insulating layers 9see column 10, lines 42 et seq.).

As to **claim 7**, Hayashida et al. teach a portion of the substrate being sandwiched by the mold, as shown in figure 1.

As to **claim 8**, Hayashida et al. teach the circuit element on the substrate to be a semiconductor chip 10, as shown in figure 1.

As to **claim 11**, Lee et al. teach an air vent "striding" over a peripheral part of the cavity, and the air vent extends from inside the cavity to outside the cavity, as can be plainly seen in figures 1, 3, 6,11 or 14.

As to **claims 12 and 13**, Lee et al. teach bringing the back face of the planar body into contact with the lower mold which has air vents, and the planar body contacts at least one of the air vents (see figure 1) and air is released through the air vents (see col. 1, lines 65-67, continued to col. 2, lines 1-4).

Allowable Subject Matter

Claims 3, 5, 9 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

the planar body being a conductive foil, which has a surface provided with conductive patterns formed in convex shape by separation grooves as recited in claim 3;

air vents disposed in parallel as recited in claim 5;

a plurality of blocks are aligned, and within each block are conductive patterns forming a plurality of mounting portions that re arranged in a matrix form on the substrate as recited in claim 9;

bringing the back face of the planar body into contact with the lower mold and sealing at least one of the air vents with the back face of the planar body as recited in claim 14.

Claim 6 is dependent upon claim 5; claim 10 is dependent upon claim 9.

Response to Arguments

Applicant's arguments filed July 11th, 2005 have been fully considered but they are not persuasive. The applicant has argued that neither Hayashida et al. nor Lee et al. teach mounting the circuit elements (i.e. chips) on conductive patterns. However, Hayashida et al. does teach mounting chips on conductive patterns as evidenced by figure 21 of Hayashida et al. which shows flip-chip bonding. Also, the applicant has argued that neither Hayashida et al. nor Lee et al. teach air vents in a lower mold to allow for air to escape and avoid warping of the planar body during resin sealing.

However, Lee et al. teach an upper and lower mold, wherein the lower mold at least has air vents, and Hayashida et al. also teach an upper and lower mold. Lee et al. is combined with Hayashida et al. to reject claim 1, with the obvious advantage of allowing air to escape which is detailed in the rejection of claim 1 above. Neither Lee et al. nor Hayashida et al. expressly teach avoiding warpage of the planar body (i.e. the substrate). However, the applicant should note that this is not a limitation included in claim 1. Even if the limitation of avoiding warpage was in claim 1, it would be viewed as result language and not be given any appreciable weight.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action (*specifically the amendment to independent claim 1 and the addition of three new claims*). Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/20/05

Scott Geyer
July 20, 2005